Amendments to the Claims:

1. (currently amended) A transmission circuit that receives input data at a first rate and outputs data at a second rate, the transmission circuit comprising:

a processor for controlling operations of the transmission circuit, the processor ~~capable of~~ for accepting input data and generating corresponding first data having a plurality of bits; and

a format converting circuit electrically connected to the processor for generating second data having a plurality of bits according to the first data, the format converting circuit comprising:

a plurality of input units each for receiving one bit of the first data;

a plurality of output units each for outputting one bit of the second data after receiving the bit; and

a bit control circuit electrically connected between the input units and the output units for generating bits outputted by the output units according to bits received from the input units;

the bit control circuit transmitting a bit received by an input unit to an output unit without having the bit passing through other input and output units, a number of bits between the bit received by the input unit and a most significant bit of the first data being different from a number of bits between the bit outputted by the output unit and a most significant bit of the second data;

wherein the processor further controls the transmission circuit to output data sequentially according to the second data ,and the bit control circuit further comprises an operating circuit electrically connected between the input units and the output units for performing a logical operation according to a predetermined law on the bits received by the input units to generate the bits transmitted by the output units.

2. (currently amended) The transmission circuit of claim 1 wherein the processor is for ~~capable of~~ buffering the first or second data so that the processor outputs data at a second rate according to the second data.

3. (cancelled)

4. (original) The transmission circuit of claim 1 wherein the bit control circuit further comprises a bit transmission circuit for transmitting a bit of predetermined data to an output unit.

5. (currently amended) The transmission circuit of claim 1 wherein the bit control circuit is for ~~capable of~~ transmitting two bits received from two different input units to two different output units separately.

6. (original) The transmission circuit of claim 1 further comprising a bus connected between the processor and the format converting circuit for transmitting the data between the processor and the format converting circuit.

7. (currently amended) The ~~A~~ transmission circuit of claim 1, wherein the

transmission circuit is used for realizing a rate adaptation layer of a digital communication system~~, the transmission circuit receiving input data at a first rate and according to the input data generating output data at a second rate, the transmission circuit comprising:~~

~~a processor for controlling operations of the transmission circuit, the processor capable of for accepting the input data and generating corresponding first data having a plurality of bits; and~~

~~a format converting circuit electrically connected to the processor for generating second data according to the first data and a converting control signal from the processor, and transmitting the second data to the processor;~~

~~wherein the processor generates an output signal at the second rate according to the second data~~.

8. (cancelled)

9. (cancelled)

10. (cancelled)

11. (cancelled)

12. (cancelled)

13. (cancelled)